

# KA3842AC/KA3842AE SMPS Controller

## Features

- Low start current 0.2mA (Typ.)
- Operating range up to 500kHz
- Cycle by cycle current limiting
- Under Voltage Lock Out (UVLO) with hysteresis
- Short shutdown delay time: Typ.100ns
- High current totem-pole output
- Output swing limiting: 22V

## Description

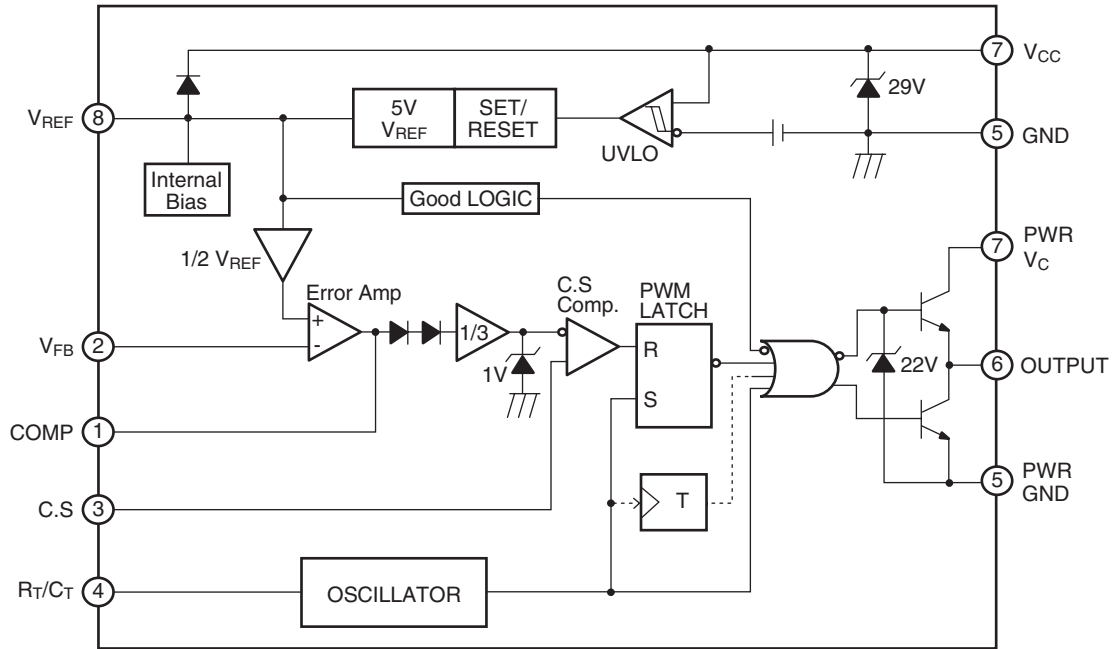
The KA3842AC/KA3842AE are fixed PWM controllers for Off Line and DC to DC converter applications. The internal circuits include UVLO, low start up current, temperature compensated reference, high gain error amplifier, current sensing comparator, and high current totem pole output for driving a POWER MOSFET. Also KA3842AC/KA3842AE provides low start up current below 0.3mA and short shutdown delay time, typically 100ns. The KA3842AC/KA3842AE has a UVLO threshold of 16V(on) and 10V(off). The KA3842AC/KA3842AE can operate within a 100% duty cycle.



## Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method
KA3842AC	-0 to +70°C	Yes	8-DIP	Tube
KA3842AE				

Internal Block Diagram



## Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	30	V
$I_O$	Output Current	$\pm 1$	A
$V_{I(ANA)}$	Analog Inputs (Pins 2, 3)	-0.3 to 6.3	V
$I_{SINK(EA)}$	Error Amp. Output Sink Current	10	mA
$P_D$	Power Dissipation	1	W
$R\theta_{ja}$	Thermal Resistance, Junction-to-Air <sup>(4)</sup>	95	$^{\circ}C/W$

## Electrical Characteristics

( $V_{CC} = 15V$ ,  $R_T = 10k^{\frac{3}{4}}$ ,  $C_T = 3.3nF$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>REFERENCE SECTION</b>						
$V_{REF}$	Output Voltage	$T_J = 25^{\circ}C$ , $I_O = 1mA$	4.9	5.0	5.1	V
$\Delta V_{REF}$	Line Regulation	$V_{CC} = 12V$ to $25V$	–	6	20	mV
	Load Regulation	$I_O = 1mA$ to $20mA$	–	6	25	mV
$I_{SC}$	Output Short Circuit	$T_A = 25^{\circ}C$	–	-100	-180	mA
<b>OSILLATOR SECTION</b>						
$F_{OSC}$	Initial Accuracy	$T_J = 25^{\circ}C$	47	52	57	kHz
$ST_V$	Voltage Stability	$V_{CC} = 12V$ to $25V$	–	0.2	1	%
$V_{OSC}$	Amplitude	$V_{PIN4}$ , Peak to Peak	–	1.7	–	V
$I_{DISCHG}$	Discharge Current	$T_J = 25^{\circ}C$ , Pin 4 = 2V	7.8	8.3	8.8	mA
<b>CURRENT SENSE SECTION</b>						
$G_V$	Gain <sup>(2)(3)</sup>		2.85	3	3.15	V/V
$V_{I(MAX)}$	Maximum Input Signal <sup>(2)</sup>	$V_{PIN1} = 5V$	0.9	1.0	1.1	V
PSRR	PSRR <sup>(1)(2)</sup>	$V_{CC} = 12V$ to $25V$	–	70	–	dB
$I_{BIAS}$	Input Bias Current		–	-2	-10	$\mu A$
$T_D$	Delay to Output <sup>(1)</sup>	$V_{PIN3} = 0V$ to $2V$	–	100	200	ns
<b>ERROR AMPLIFIER SECTION</b>						
$V_I$	Input Voltage	$T_{PIN1} = 2.5V$	2.42	2.50	2.58	V
$I_{BIAS}$	Input Bias Current		–	-0.3	-2	$\mu A$
$G_{VO}$	Open Loop Gain <sup>(1)</sup>	$V_O = 2V$ to $4V$	65	90	–	dB
GBW	Unity Gain Bandwidth <sup>(1)</sup>	$T_J = 25^{\circ}C$	0.7	1	–	MHz
PSRR	PSRR <sup>(1)</sup>	$V_{CC} = 12V$ to $25V$	60	70	–	dB
$I_{SINK}$	Output Sink Current	$V_{PIN2} = 2.7V$ $V_{PIN1} = 1.1V$	2	6	–	mA
$I_{SOURCE}$	Output Source Current	$V_{PIN2} = 2.3V$ $V_{PIN1} = 5.0V$	-0.5	-0.8	–	mA
$V_{OH}$	Output High Voltage	$V_{PIN2} = 2.3V$ , $R1 = 15k^{\frac{3}{4}}$ to GND	5	6	–	V
$V_{OL}$	Output Low Voltage	$V_{PIN2} = 2.7V$ $R1 = 15k^{\frac{3}{4}}$ to Pin 8	–	0.8	1.1	V

**Electrical Characteristics** (Continued)(V<sub>CC</sub> = 15V, R<sub>T</sub> = 10k<sup>3/4</sup>, C<sub>T</sub> = 3.3nF, T<sub>A</sub> = 0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>OUTPUT SECTION</b>						
V <sub>OL</sub>	Output Low Level	I <sub>SINK</sub> = 20mA	–	0.1	0.4	V
		I <sub>SINK</sub> = 200mA	–	1.5	2.2	V
V <sub>OH</sub>	Output High Level	I <sub>SOURCE</sub> = 20mA	13	13.5	–	V
		I <sub>SOURCE</sub> = 200mA	12	13.5	–	V
t <sub>R</sub>	Rise Time <sup>(1)</sup>	T <sub>J</sub> = 25°C, C <sub>1</sub> = 1nF	–	40	100	ns
t <sub>F</sub>	Fall Time <sup>(1)</sup>	T <sub>J</sub> = 25°C, C <sub>1</sub> = 1nF	–	40	100	ns
V <sub>OLIM</sub>	Output Voltage Swing Limit	V <sub>CC</sub> = 27V, C <sub>1</sub> = 1nF	–	22	–	V
<b>UNDER VOLTAGE LOCKOUT SECTION</b>						
V <sub>TH</sub>	Start Threshold		15	16	17	V
V <sub>TL</sub>	Min. Operating Voltage (After turn on)		9	10	11	V
<b>PWM SECTION</b>						
D <sub>MAX</sub>	Maximum Duty Cycle		94	96	100	%
D <sub>MIN</sub>	Minimum Duty Cycle		–	–	0	%
<b>TOTAL STANDBY CURRENT</b>						
I <sub>ST</sub>	Start-Up Current		–	0.2	0.4	mA
I <sub>CC</sub>	Operating Supply Current	V <sub>PIN2</sub> = V <sub>PIN3</sub> = 0V	–	11	17	mA
V <sub>Z</sub>	V <sub>CC</sub> Zener Voltage	I <sub>CC</sub> = 25mA	–	29	–	V

\* Adjust V<sub>CC</sub> above the start threshold before setting at 15V**Notes:**

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with V<sub>2</sub> = 0V.
3. Gain defined as:  $G_V = \Delta V_{PIN1} / \Delta V_{PIN3}$  (V<sub>PIN3</sub> = 0 to 0.8V)
4. Junction-to-air thermal resistance test environments

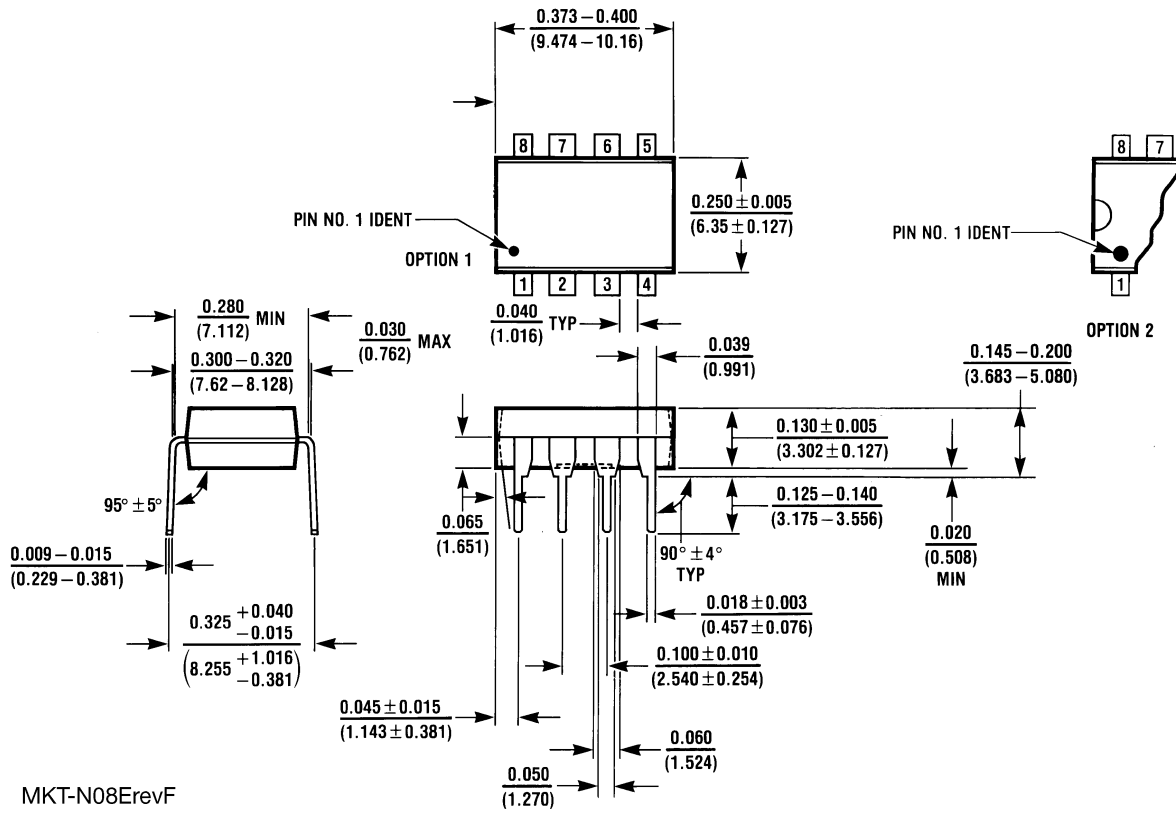
## PCB information:

Board thickness; 1.6mm, Board dimension: 76.2 X 114.3mm<sup>2</sup>, Ref.: EIA/JSED51-3 and EIA/JSED51-7  
 Board structure; Using the single layer PCB.

# Package Dimensions

## 8-Pin DIP

Dimensions in millimeters



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|---|---|

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